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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DAVIDSON, DAN	
ART UNIT	**PAPER NUMBER**
2627	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/994,009	HEYDARI ET AL.	
	Examiner	Art Unit	
	Dan I. Davidson	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30 and 32-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30 and 32-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02092007; 07052007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The information disclosure statements filed February 9, 2007 and July 5, 2007 have been received and have been considered and made of record.

Claim Objections

2. Claims 16, 24, and 30 are objected to because of the following informalities:

(1) In claim 16, line 6, "third" should be replaced with --second--.

(2) In claim 24, line 4, the second instance of "first" should be deleted.

(3) In claim 30, line 2, "words" should be replaced with --bits--.

(4) In claim 30, line 3, "word" should be replaced with --symbol--.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-9 and 32-34 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 1-9 and 32-34 are drawn to a coded binary sequence which does not fall under one of the four enumerated categories of patentable subject matter recited in section 101 (process, machine, manufacture, or composition of matter). Furthermore, the coded binary sequence is an abstract idea that fails to produce a useful, tangible, and concrete result.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-9 and 32-34 are rejected under 35 U.S.C. 101 because the claimed invention is not supported by either a specific and substantial asserted utility or a well established utility. See the 35 U.S.C. 101 rejection above.

Claims 1-9 and 32-34 are also rejected under 35 U.S.C. 112, first paragraph. Specifically, since the claimed invention is not supported by either a specific and substantial asserted utility or a well established utility for the reasons set forth above, one skilled in the art clearly would not know how to use the claimed invention.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 11-13 and 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The preamble in claims 11-13 is drawn to a Viterbi detector, thereby indicating that the claim is an apparatus claim. However, there are no structural limitations in any of claims 11-13.

The last limitation in claim 28 is not understood by the Examiner. What is the difference between the lengths of the first and second code symbols and the number of the code bits?

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-8, 10-23, 27-28, 30, and 32-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Kuki et al (US 6,233,715 B1).

Re claim 1; Kuki et al disclose a coded binary sequence, comprising: a first group of consecutive bits, the first group having first and second separate (i.e. nonoverlapping) portions and representing one of logic 1 and a logic 0, the bits in the first portion each having a first state and the bits in the second portion each having a second state (col. 6, Table II, Case 6, NRZI Encoded Data "1"); and a second group of consecutive bits separate from the first group and each having a same state, the second group representing only the other of the logic 1 and the logic 0 (col. 6, Table II, Case 6, NRZI Encoded Data "0").

Re claims 2 and 7; Kuki et al disclose that the first and second portions of the first group (which is the second group in claim 7) respectively comprise first and second halves of the first group (col. 6, Table II, Case 6, NRZI Encoded Data "1").

Re claim 3; Kuki et al disclose that the first and second groups respectively represent logic 1 and logic 0 (col. 6, Table II, Case 6, NRZI Encoded Data "1", "11" and "00" respectively represent logic 1 and logic 0).

Re claim 4; the limitations at this claim are met based on the sections of Kuki et al cited above in the rejection of claim 1.

Re claim 5; Kuki et al disclose that the first and second groups respectively represent logic 0 and logic 1 (see the rejection of claim 1 above); the bits of the first group each have a state of logic 0 (col. 6, Table II, Case 6, NRZI Encoded Data "0"); and the first and second states respectively equal logic 1 and logic 0 (col. 6, Table II, Case 6, NRZI Encoded Data "1").

Re claim 6; Kuki et al disclose that the first and second groups each respectively comprise four consecutive bits (col. 6, Table II, Case 6).

Re claim 8; these claim limitations are met by Kuki et al based on the sections of Kuki et al cited in the rejections of claims 4-6.

Re claims 10, 16, and 19; Kuki et al disclose a disk drive system comprising: a storage disk (Fig. 1, 12) having disk sectors operable to store application data (Fig. 2, data sectors); and servo wedges that store servo data (Fig. 2, servo sectors) that includes the format claimed in claim 10 (which is equivalent to the coded binary sequence of claim 1) (Fig. 2, 66; Table II, Gray Code). It is inherent in Kuki et al that there be a motor coupled to and operable to rotate the disk given that the disk is rotating as shown in Figure 1. Kuki et al further disclose a read/write head operable to generate a servo signal that represents the servo data and having a position with respect to the

surface of the storage disk (Fig. 1, 14); a read-head positioning circuit operable to move the read head over the surface of the disk (Fig. 1, 34); and a servo circuit coupled to the read head and operable to recover the servo data from the servo signal (Fig. 1, 30, 32).

Re claims 11-13; Kuki et al disclose a Viterbi detector (Fig. 1, 28) operable to: receive a signal that represents a coded binary sequence as claimed in claims 11-13 (which is equivalent to the coded binary sequence of claims 1 and 4); and recover the binary sequence from the signal (Fig. 7, 1/4 Code, EPR4EQ, EPR4Viterbi w/ECU).

Re claims 14 and 17; Kuki et al disclose a servo circuit, comprising: a sample circuit operable to generate samples of a signal that represents a coded binary sequence as claimed in claim 14 (which is equivalent to the coded binary sequence of claims 1 and 4) (Fig. 1, 22); and a Viterbi detector coupled to the sample circuit and operable to recover the coded binary sequence from the samples of the signal (see the rejection of claims 11-13 above).

Re claims 15 and 18; it is inherent in Kuki et al that there be a decoder coupled to the Viterbi detector operable to decode the recovered binary sequence since data that is encoded as Gray code data of necessity must be decoded once a Viterbi detector has detected the Gray code data.

Re claims 20 and 23; Kuki et al disclose a method, comprising: coding one of a logic 1 and a logic 0 as a first group of consecutive bits, the first group having first and second equally sized portions that respectively comprise first and second halves of the first group, the bits in the first portion each having a first state and the bits in the second portion each having a second state (col. 6, Table II, Case 6, NRZI Encoded Data "1");

and coding the other and only the other of the logic 1 and the logic 0 as a second group of consecutive bits separate from the first group and each having a same state (col. 6, Table II, Case 6, NRZI Encoded Data "0").

Re claim 21; Kuki et al disclose that the first and second groups respectively represent a logic 1 and a logic 0 (col. 6, Table II, Case 6, NRZI Encoded Data "1"; "11" and "00" respectively represent a logic 1 and a logic 0); the first and second states respectively equal logic 0 and logic 1 (col. 6, Table II, Case 6, NRZI Encoded Data "1"); and the same state equals a logic 0 (col. 6, Table II, Case 6, NRZI Encoded Data "0").

Re claim 22; Kuki et al disclose coding the one of the logic 1 and the logic 0 as a first group of four consecutive bits; and coding the other of the logic 1 and the logic 0 as a second group of four consecutive bits (col. 6, Table II, Case 6).

Re claim 27; Kuki et al disclose a method, comprising: writing a first code symbol into a servo wedge of a data-storage disk (Fig. 2, Servo, 66), the first code symbol having a first group of code bits and a second group of code bits, having a length and representing one of a logic 1 and a logic 0, each bit in the first group having a first value and each bit in the second group having a second value that is different than the first value (col. 6, Table II, Case 6, NRZI Encoded Data "1"); and writing a second code symbol into the servo wedge, the second code symbol having the length or approximately the length, having a single group of code bits each having the same value, and representing only the other of the logic 1 and the logic 0 (col. 6, Table II, Case 6, NRZI Encoded Data "0").

Re claim 28; Kuki et al disclose that the first and second code symbols each comprise a number of the code bits (col. 6, Table II, Case 6, 4 code bits); and the lengths of the first and second code symbols (i.e. 4 code bits) are each less than the product of the number and a length of a servo-bit region (col. 6, Table II, Case 6).

Re claim 30; Kuki et al disclose that each of the first and second groups of code bits is or is approximately half as long as the first code symbol (col. 6, Table II, Case 6, 2 bits vs. 4 bits).

Re claims 32-33; Kuki et al disclose a coded binary sequence, comprising: a first group of consecutive bits, the first group having first and second portions and representing one of a logic 1 and a logic 0, the first portion preceding the second portion, the bits in the first portion each having a first state and the bits in the second portion each having a second state (col. 6, Table II, Case 6, NRZI Encoded Data "1"); and a second group of consecutive bits each having a same state, the same state being the first state or the second state, the second group representing only the other of the logic 1 and the logic 0 (col. 6, Table II, Case 6, NRZI Encoded Data "0").

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 9, 24-26, 29, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuki et al (US 6,233,715 B1).

Re claim 9; Kuki et al disclose the limitations at claim 8 as discussed above. Kuki et al further disclose that the first and second groups respectively represent a logic 0 and a logic 1 (col. 6, Table II, Case 6). Kuki et al also disclose that the first state equals a logic 0.

However, Kuki et al do not disclose that the second and third states respectively equal a logic 0 and a logic 1; rather, Kuki et al disclose that the second and third states respectively equal a logic 1 and a logic 0. Having said that, a rearrangement of logical states without any unexpected results is not patentably distinguishing subject matter (there would be no unexpected results in this case since the logic 1 bits simply take the space of the logic 0 bits and vice versa). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to rearrange the logical states in Kuki et al to achieve the predictable result of improving the signal-to-noise ratio of the servo data (Kuki et al, col. 7, lines 21-28; specification, paragraph 2).

Re claim 24; Kuki et al disclose a method, comprising: coding a first logical bit of servo data and only the first logical bit as a first group of four consecutive bits each having a first logic level, the first logical bit representing the first logic level or a second logic level (col. 6, Table II, Case 6, NRZI Encoded Data "0"; the first logical bit represents the first logic level). Kuki et al further disclose coding a second logical bit of servo data as a second group of four consecutive bits, the second logical bit representing the first logic level if the first logical bit represents the second logic level, the second logical bit representing the second logic level if the first logical bit represents the first logic level (col. 6, Table II, Case 6, NRZI Encoded Data "1"; the first logical bit

represents the first logic level and the second logical bit represents the second logic level).

However, Kuki et al do not disclose that the second group of four consecutive bits respectively have the first logic level, the first logic level, the second logic level, and the second logic level ("0011"); rather, Kuki et al disclose that the second group of four consecutive bits respectively have the second logic level, the second logic level, the first logic level, and the first logic level ("1100"). Having said that, a rearrangement of logical states without any unexpected results is not patentably distinguishing subject matter (there would be no unexpected results in this case since the logic 1 bits simply take the space of the logic 0 bits and vice versa). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to rearrange the logical states in Kuki et al to achieve the predictable result of improving the signal-to-noise ratio of the servo data (Kuki et al, col. 7, lines 21-28; specification, paragraph 2).

Re claim 25; Kuki et al disclose that the first logical bit equals a logic 0; and the second logical bit equals a logic 1 (see the above rejection of claim 24).

Re claim 26; the limitations at this claim are met based on the discussion of claim 24 above.

Re claim 29; Kuki et al disclose the limitations at claim 27 as discussed above. Kuki et al fail to disclose that the first code symbol represents a logic 0; and the second code symbol represents a logic 1; rather, Kuki et al disclose that the first code symbol represents a logic 1; and the second code symbol represents a logic 0. Having said that, a rearrangement of logical states without any unexpected results is not patentably

distinguishing subject matter. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to rearrange the logical states in Kuki et al to achieve the predictable result of improving the signal-to-noise ratio of the servo data (Kuki et al, col. 7, lines 21-28; specification, paragraph 2).

Re claim 34; Kuki et al disclose the limitations at claim 33 as discussed above. Kuki et al further disclose that the first group represents a logic 1 (col. 6, Table II, Case 6, NRZI Encoded Data "1"); each bit of the second group has the first state (Table II, Case 6, "0000"); and the second group represents a logic 0 (Table II, Case 6, NRZI Encoded Data 0).

However, Kuki et al fail to disclose that the first state comprises a logic 0; and the second state comprises a logic 1; rather, they teach the opposite. Having said that, a rearrangement of logical states without any unexpected results is not patentably distinguishing subject matter. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to rearrange the logical states in Kuki et al to achieve the predictable result of improving the signal-to-noise ratio of the servo data (Kuki et al, col. 7, lines 21-28; specification, paragraph 2).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan I. Davidson whose telephone number is (571) 272-7552. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrea L. Wellington, can be reached on (571) 272-4483. The fax phone

number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DID
Dan I Davidson
February 13, 2008

ANDREA WELLINGTON
SUPERVISORY PATENT EXAMINER